

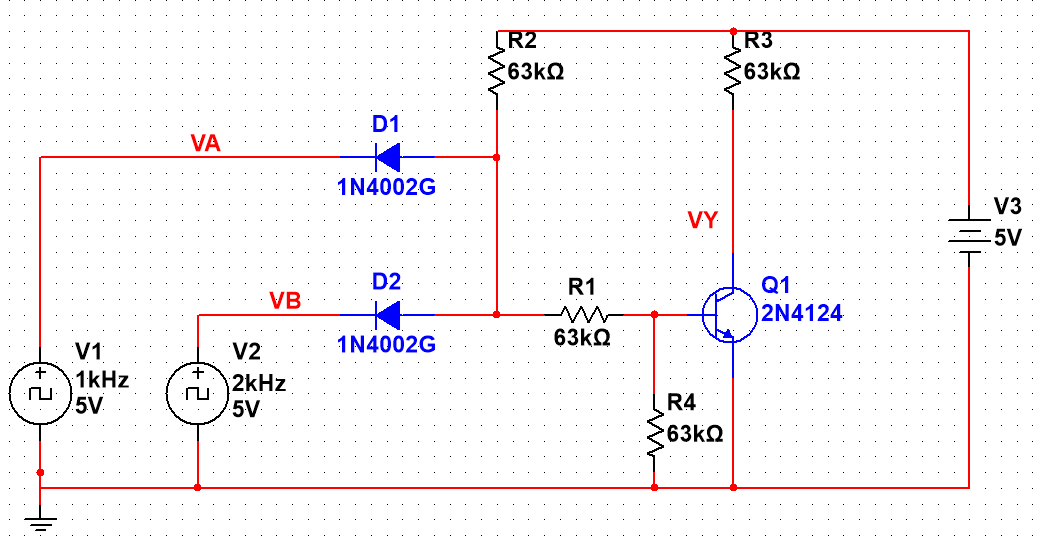
**Block Diagrams:**

Fig 1: 2 Input DTL NAND Block Diagram.

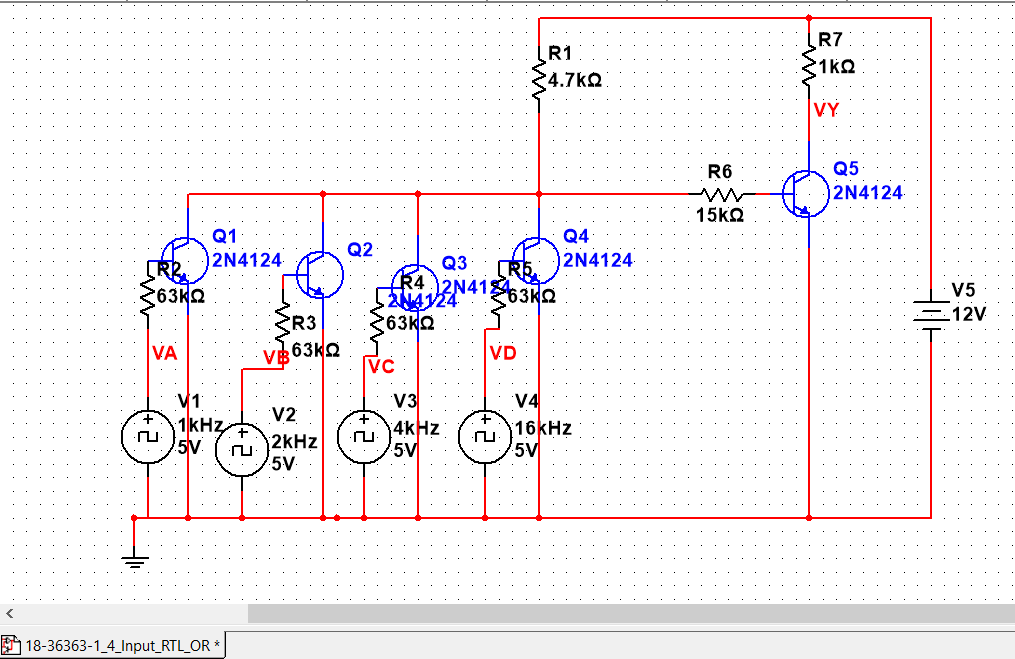
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Fig 2: 4 Input RTL OR Block Diagram.

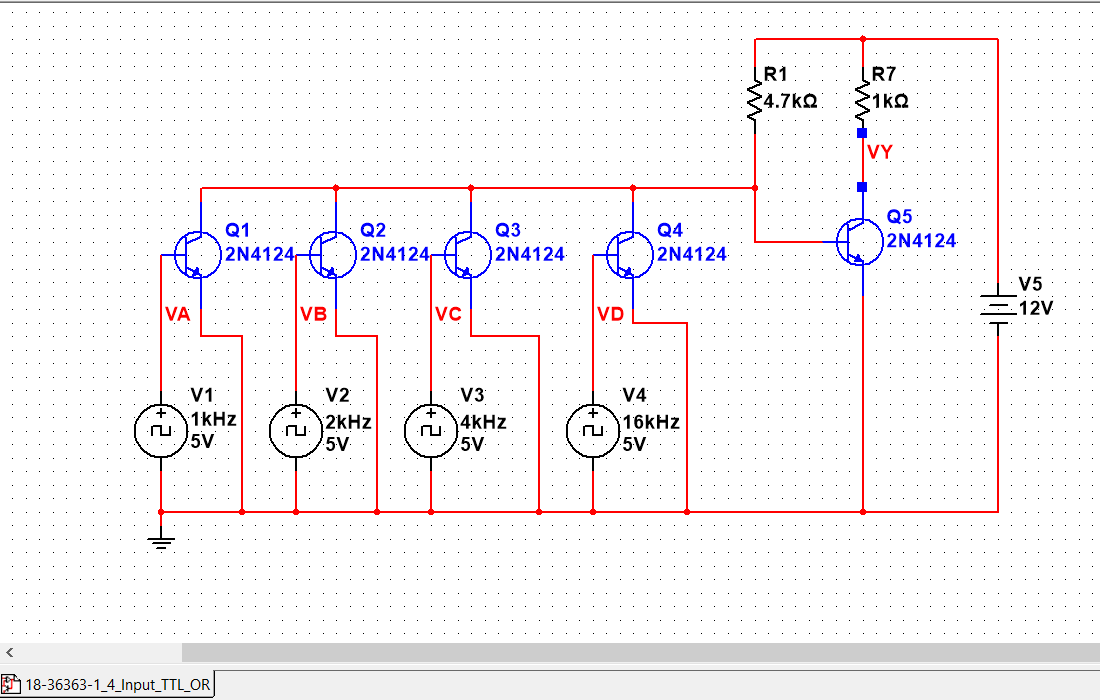


Fig 3: 4 Input TTL OR Block Diagram.

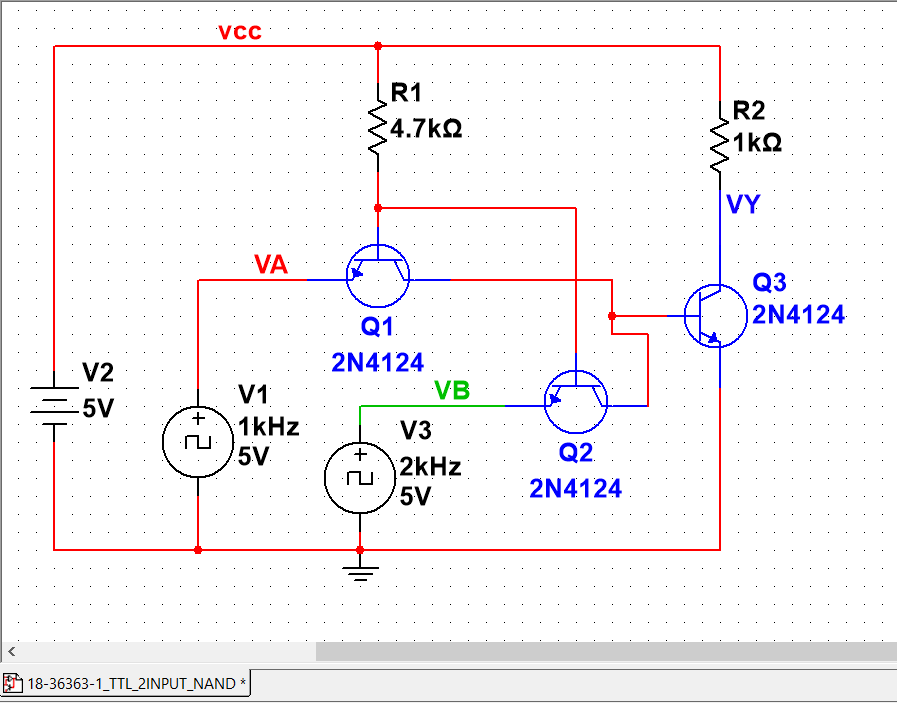
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Fig 4: 2 Input TTL NAND Block Diagram.

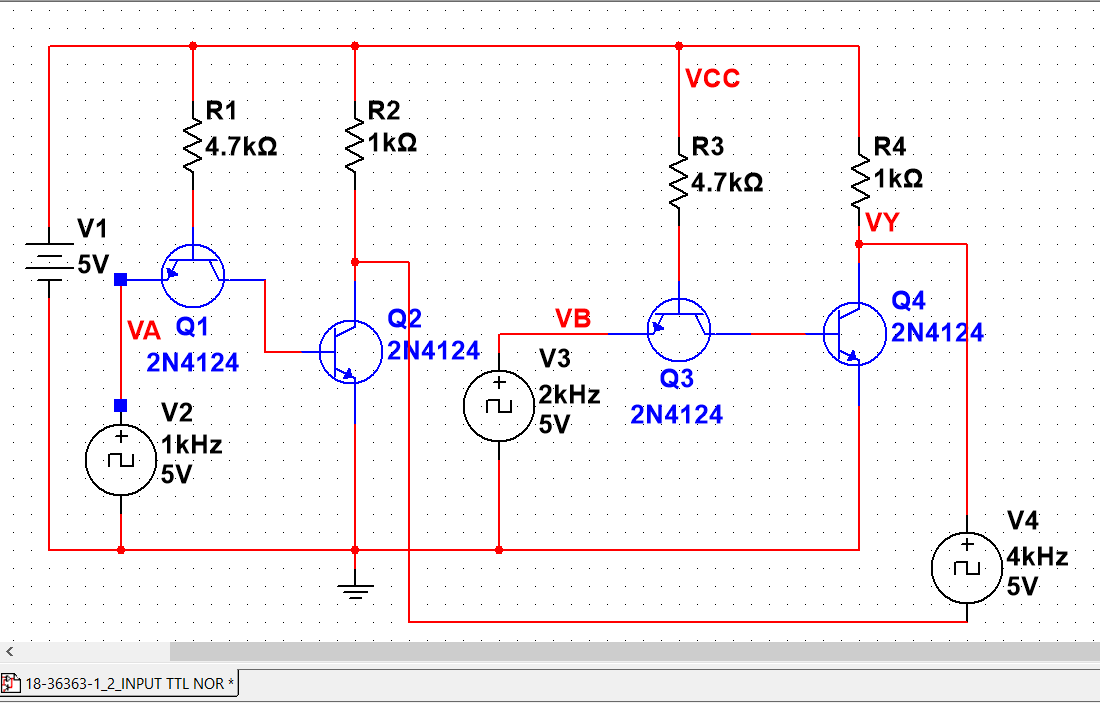


Fig 5: 2 Input TTL NOR Block Diagram.

**Graphs:**

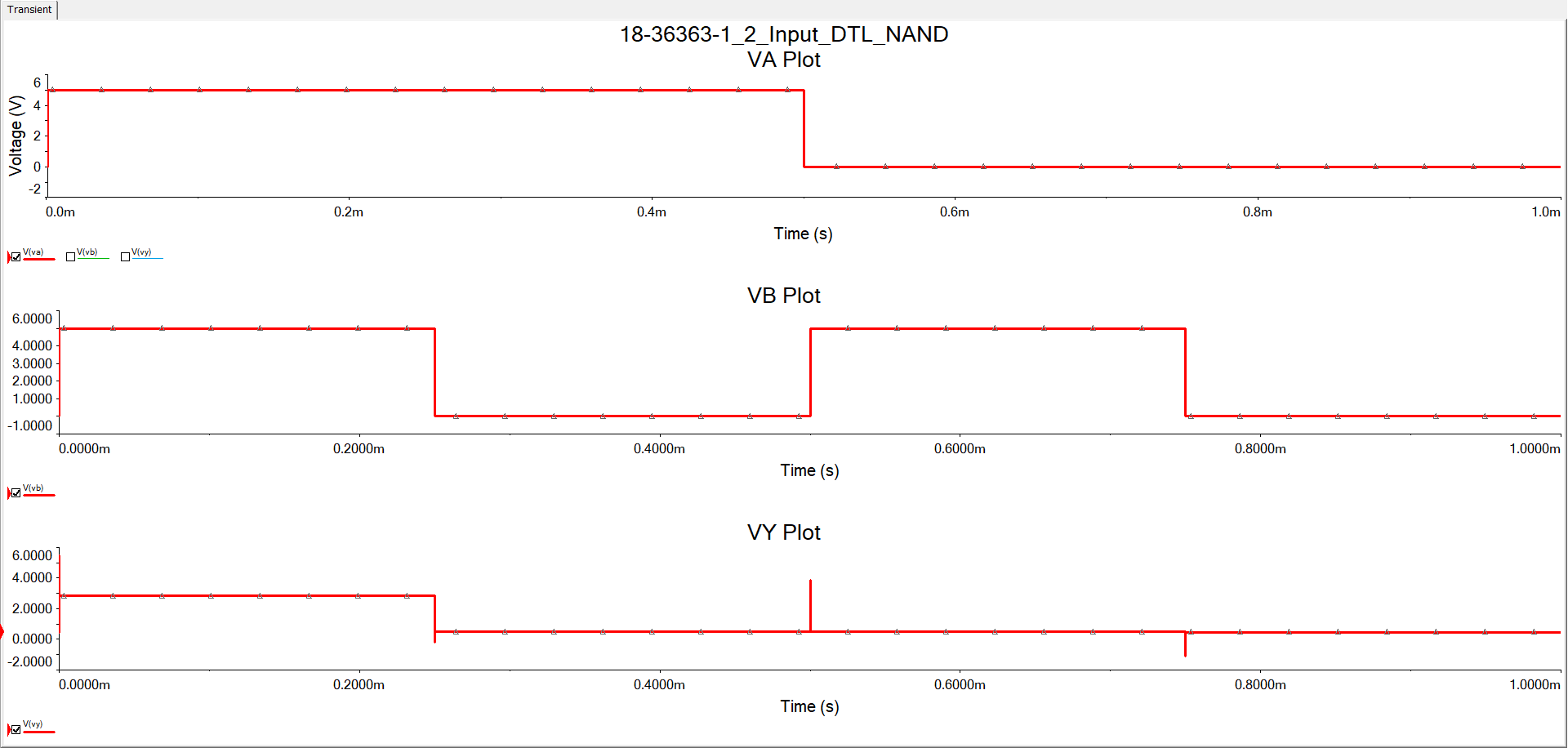
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Fig 6: 2 Input DTL NAND Graph.

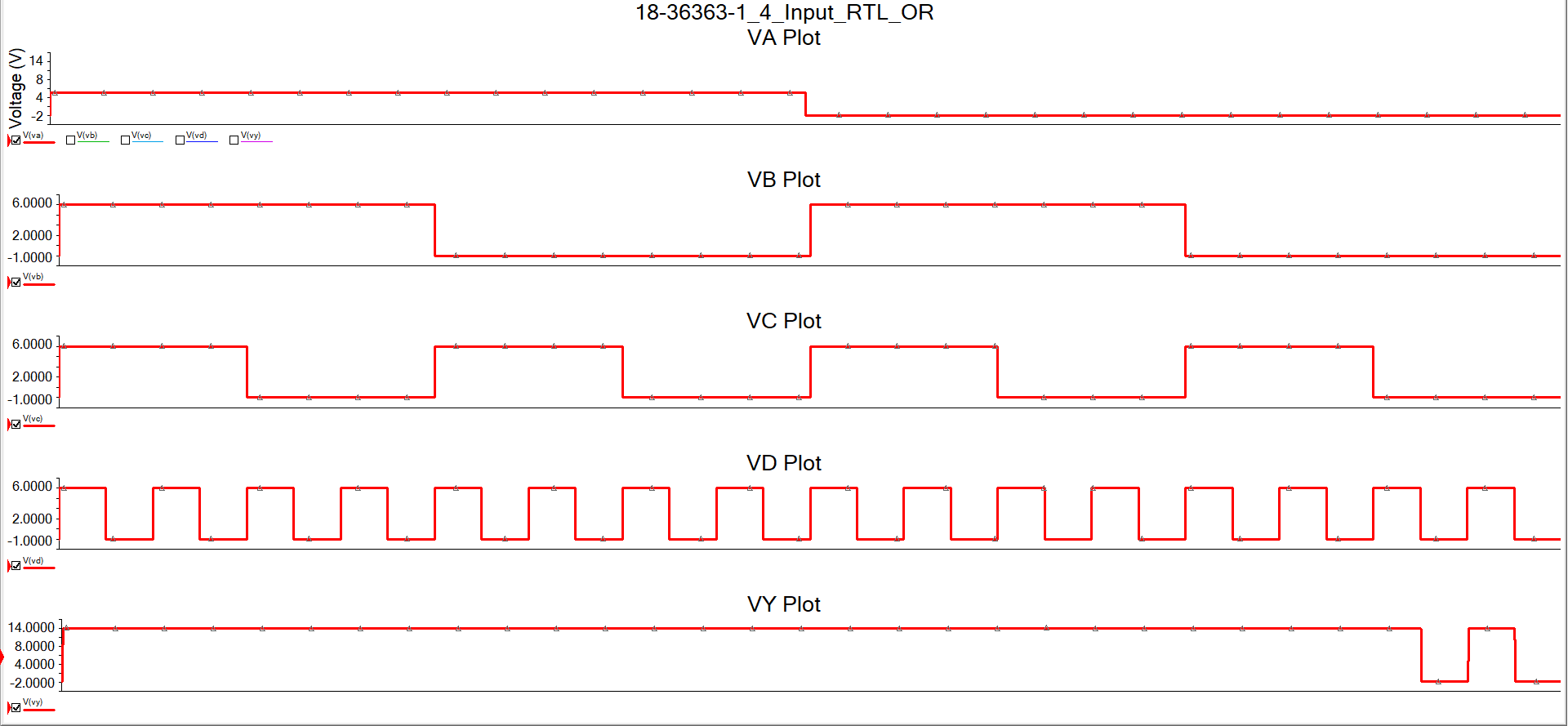


Fig 7: 4 Input RTL OR Graph.

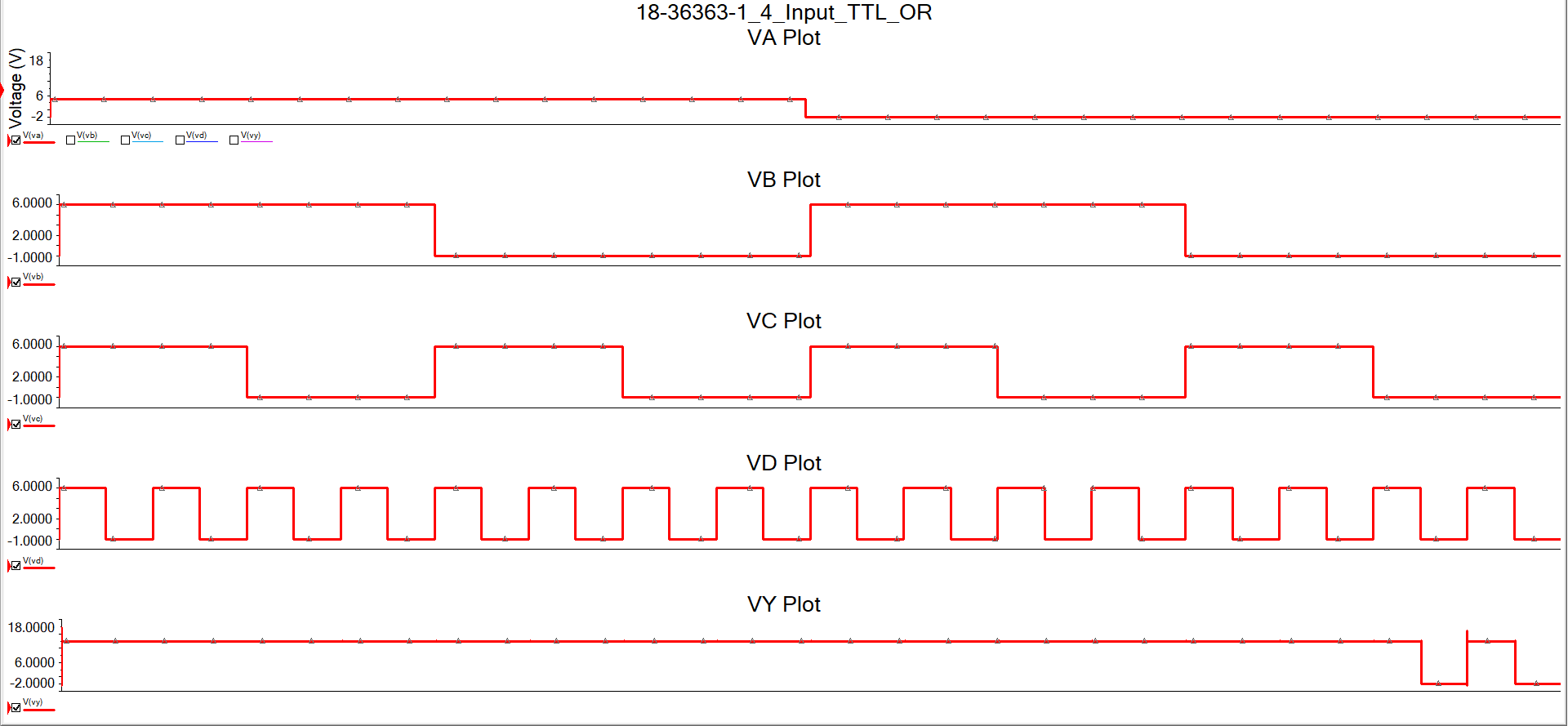


Fig 8: 4 Input TTL OR Graph.

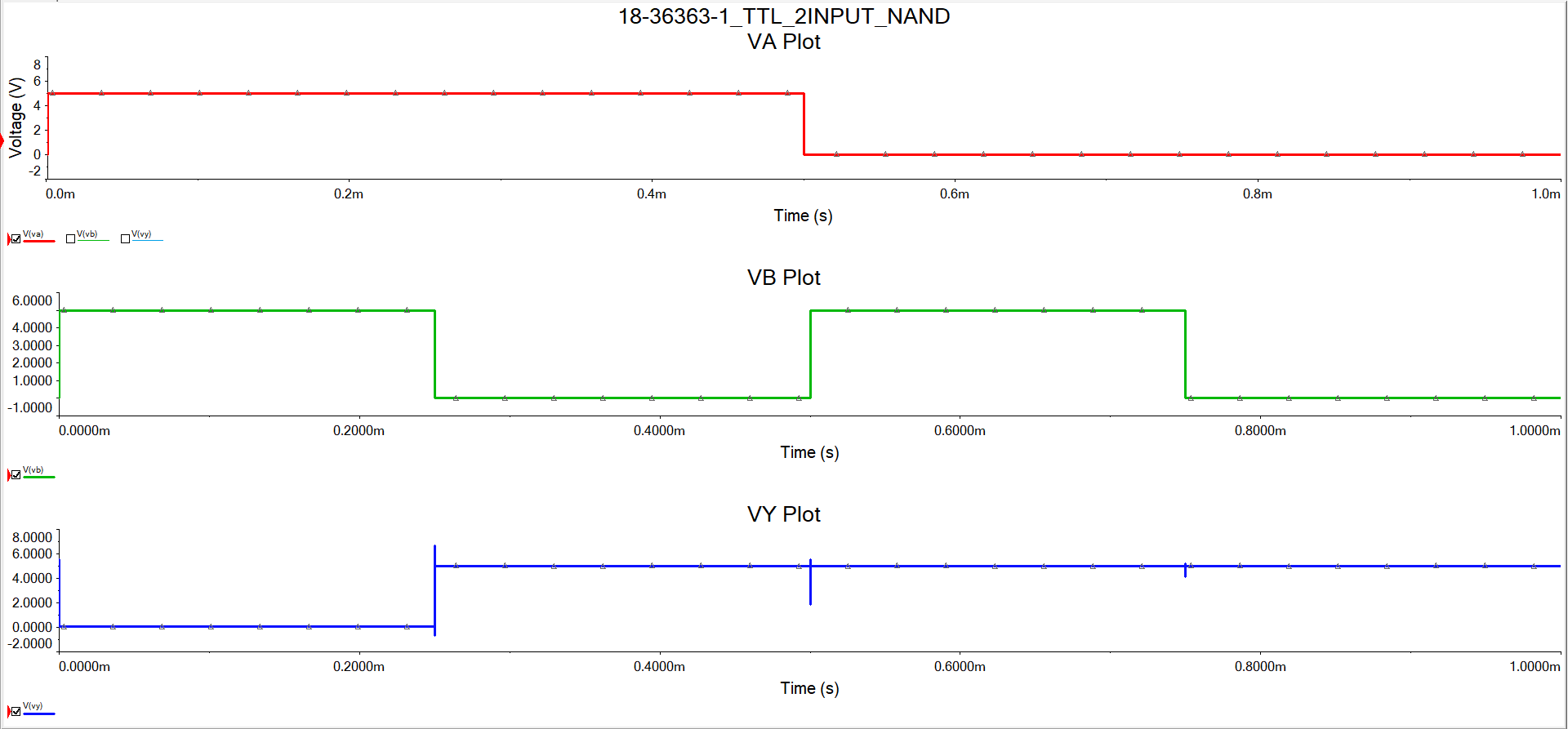


Fig 9: 2 Input TTL NAND Graph.

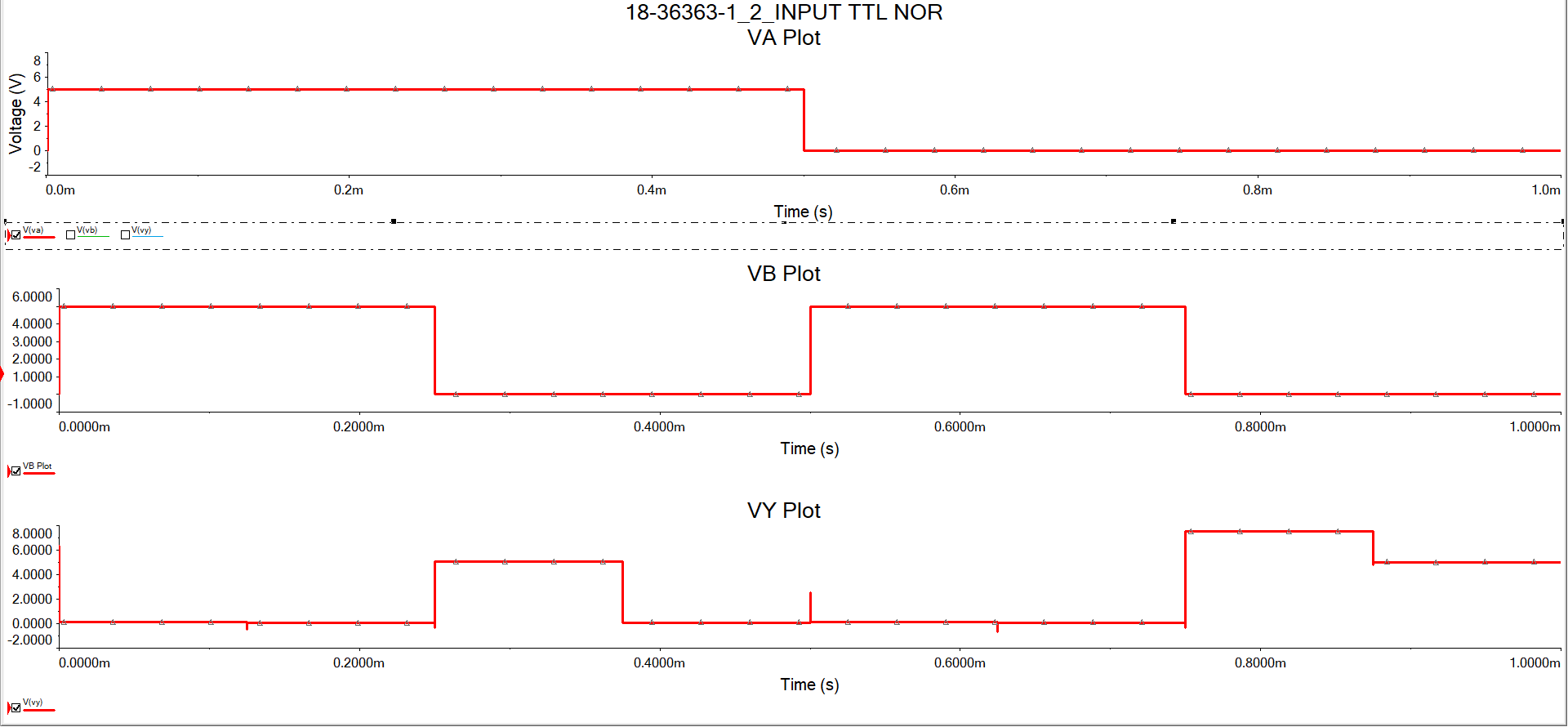


Fig 10: 2 Input TTL NOR Graph.

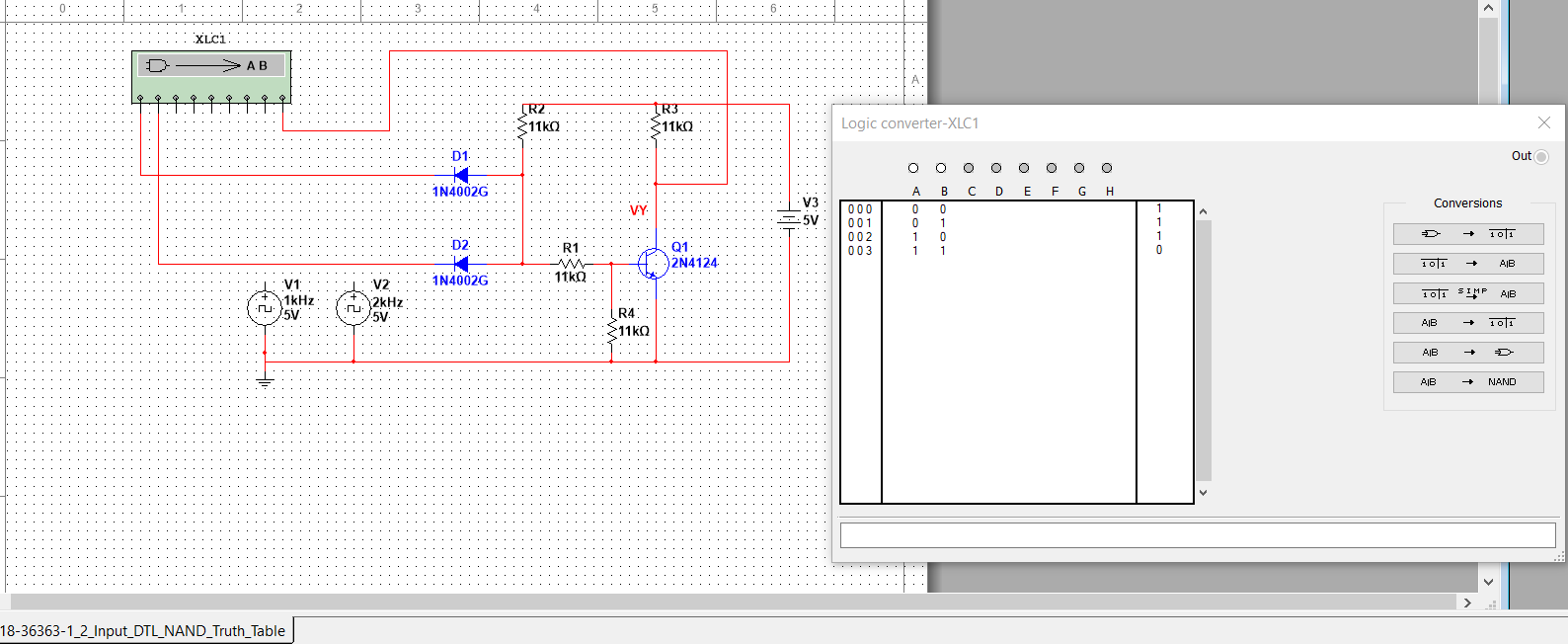
**Truth Tables:**

Fig 11: 2 Input DTL NAND Truth Table.

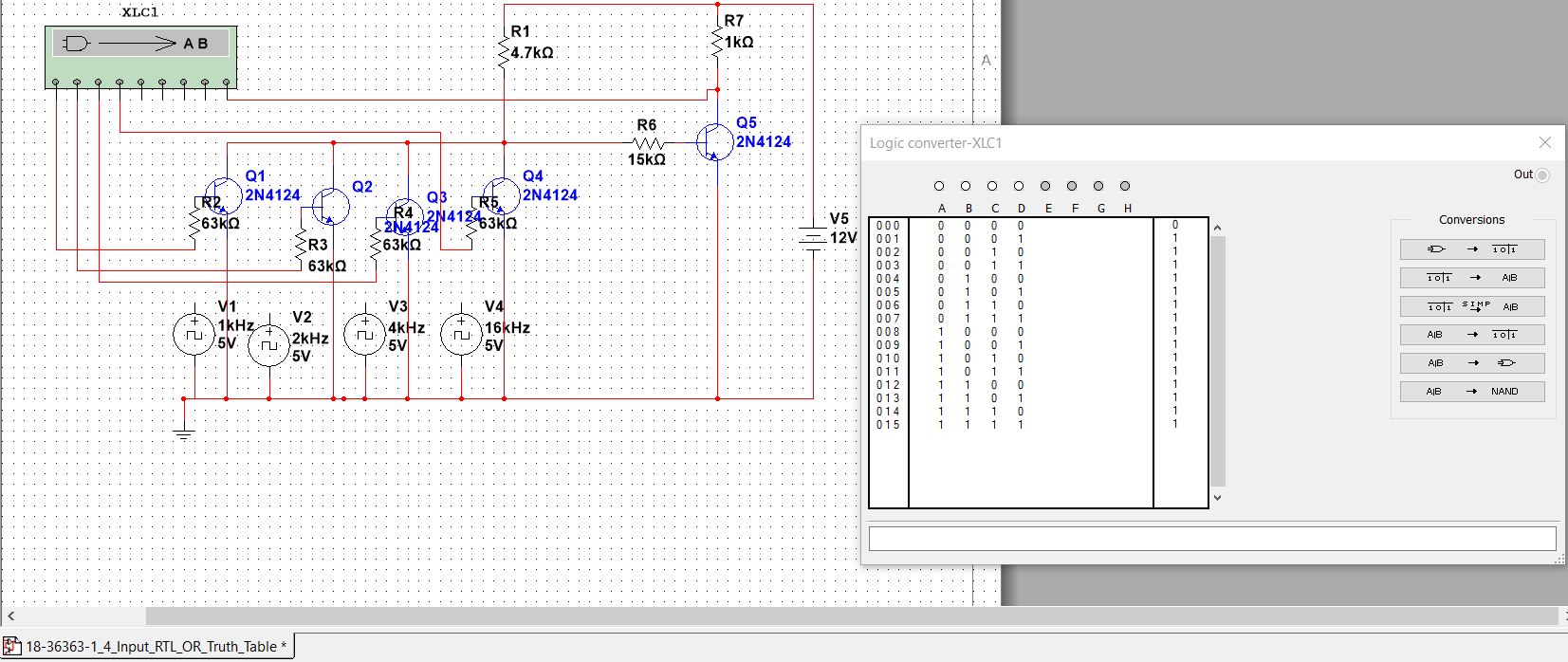


Fig 12: 2 Input RTL OR Truth Table.

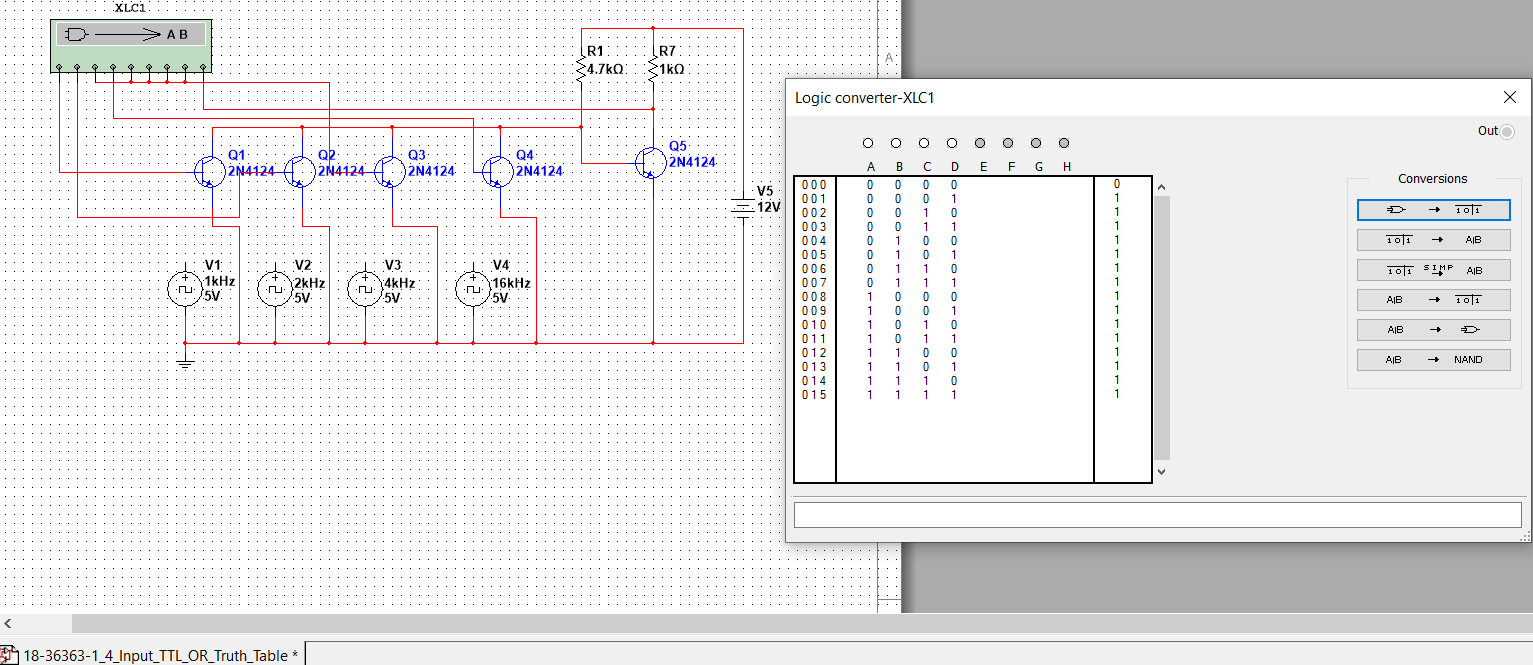


Fig 13: 4 Input TTL OR Truth Table.

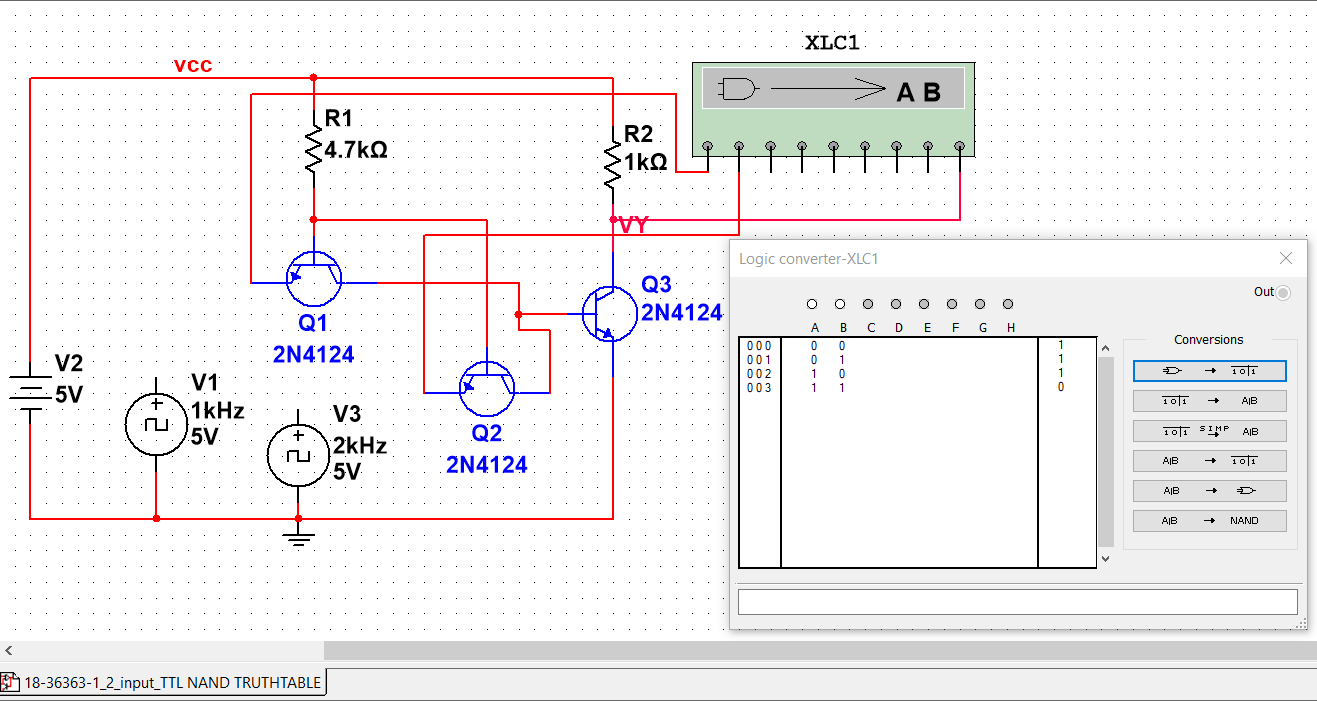


Fig 14: 2 Input TTL NAND Truth Table.

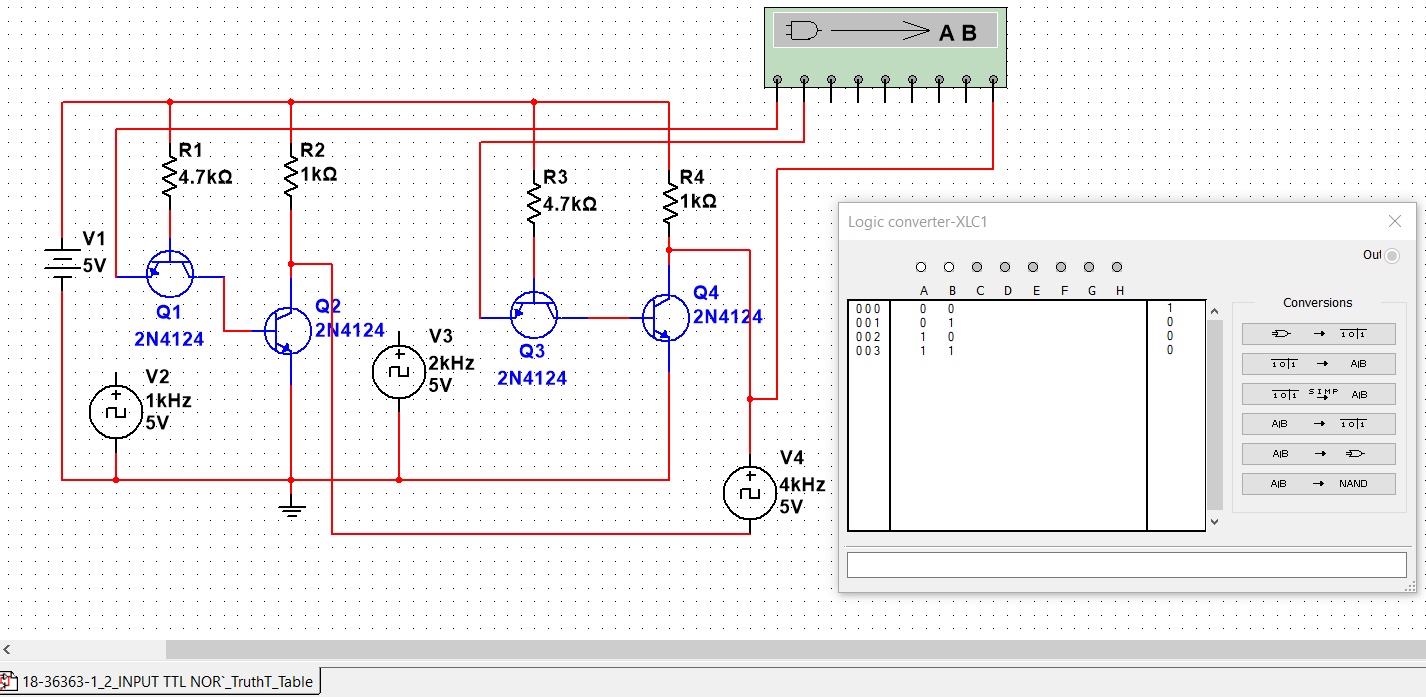


Fig 15: 2 Input TTL NOR Truth Table.